RF Locking of Femtosecond Lasers

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SLAC

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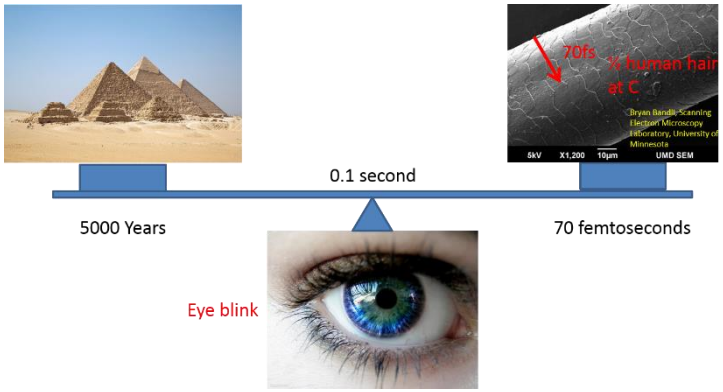
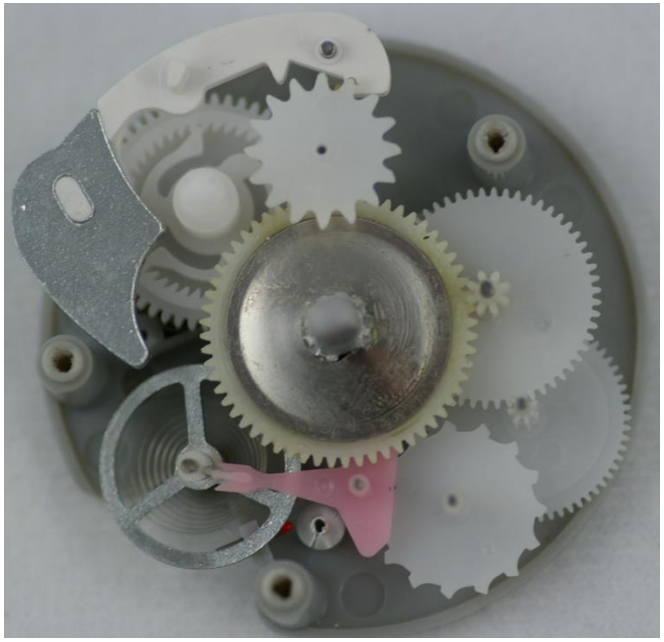
Overview

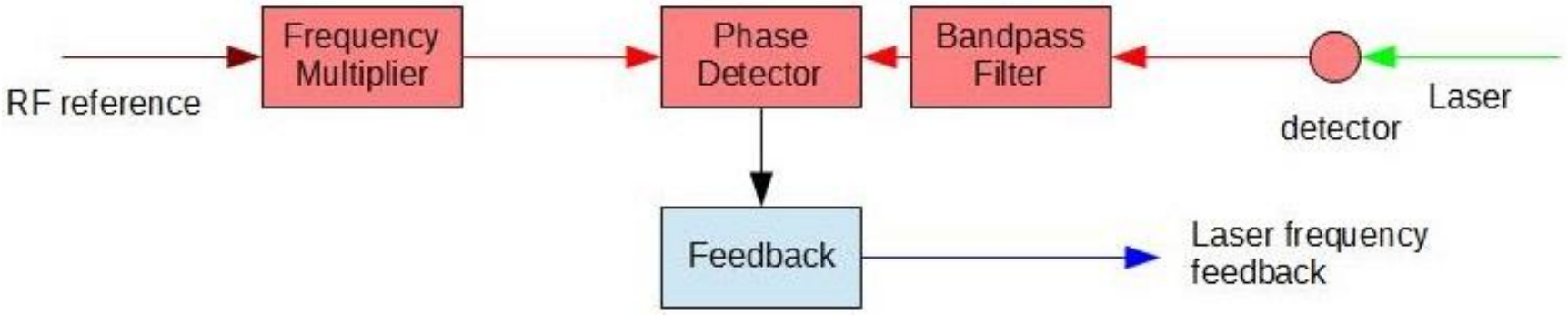




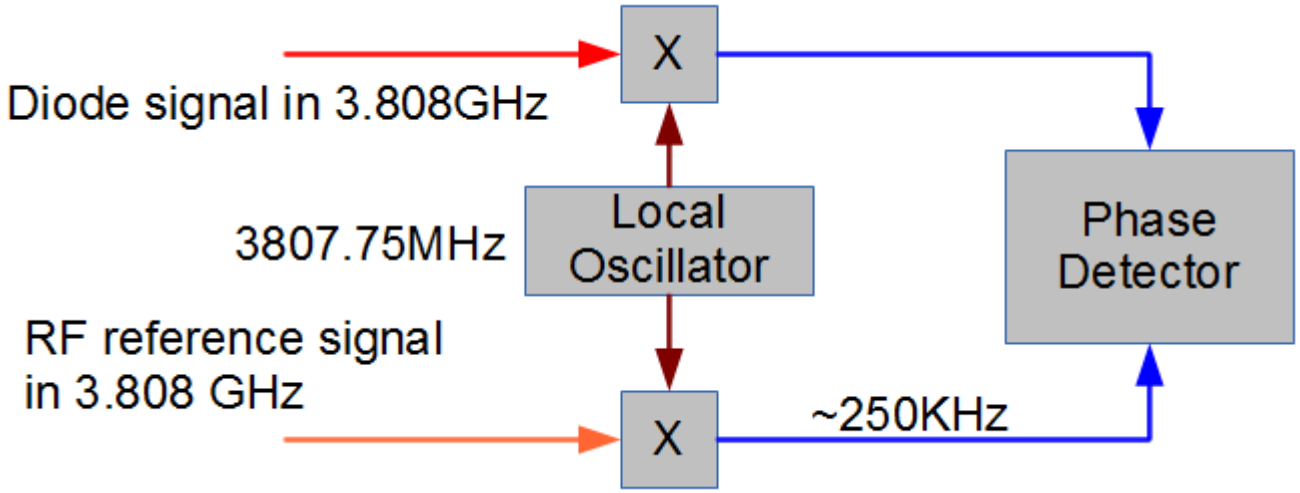
- FEIS 2013 talk discussed general laser locking concepts
- This talk is about a specific implementation
  - RF locking
  - Used at SLAC / ASTA UED system (and many other SLAC locations)
- Will discuss locking system design details that apply to other similar systems.
- RF systems good in the 10-100fs RMS range
  - We see ~25fs RMS jitter.
- **This talk is nuts and bolts hardware engineering, NO SCIENCE.**

RF locking

- Laser mode locked oscillator signal is fast (<100fs) pulses at typically ~50MHz
- Photo-diodes typically ~100ps response.
- Bandpass filter signal to get a tone at a convenient (more on this later) RF frequency ~4GHz
- Mix against a RF reference to detect phase



Heterodyne System



- Mix to an intermediate frequency rather than DC (frequencies from SLAC system)
- Low frequency phase detection much easier:
  - Can easily digitize and calculate relative phase in software
  - Can use low frequency mixer or analog multiplier with much better performance than RF mixer
- Signal levels small until RF mixer, then put gain at low frequency where cross talk is less significant.
- Technique used in radio receivers (R. Fessenden , 1901 (!!!))

RF design: Dynamic range vs Noise

- Thermal noise is -174dBm/Hz at room temperature.
  - In a typical 10KHz laser locker bandwidth, get -134dBm noise or 40 atto-watts
  - Expect RF system to get within 10dB (X10) of this noise level
- In a heterodyne system the 3rd order nonlinear terms are usually the limit. Indicated by IP3.
  - Note that depending on the device manufacturers may specify INPUT or OUTPUT IP3 – always done to make it look good!
  - Distortion in dB is 2*(PdB – IP3).
- In general it is good to roughly match noise and distortion.
  - If for example IP3 = 20dBm, noise figure = 10dB (noise -124dBm in 10KHz bandwidth) at a mixer, then a -28dBm signal will have 96dB S/N and 96dB distortion.

Laser Detectors

- ET-4000 detector: 10GHz bandwidth
- 40um active area
- IP3 not specified.
  - Bias voltage 5V: if that I represents IP3, then IP3=17dBm
  - Should measure, but haven't done so
- Used at SLAC – cheap, simple, not ideal
  - Phase depends on spot position

- Discovery Semiconductor high IP3 detector
- 20GHz, IP3 >40dBm
- Fiber coupled – takes care to match laser beam to detector
- expensive

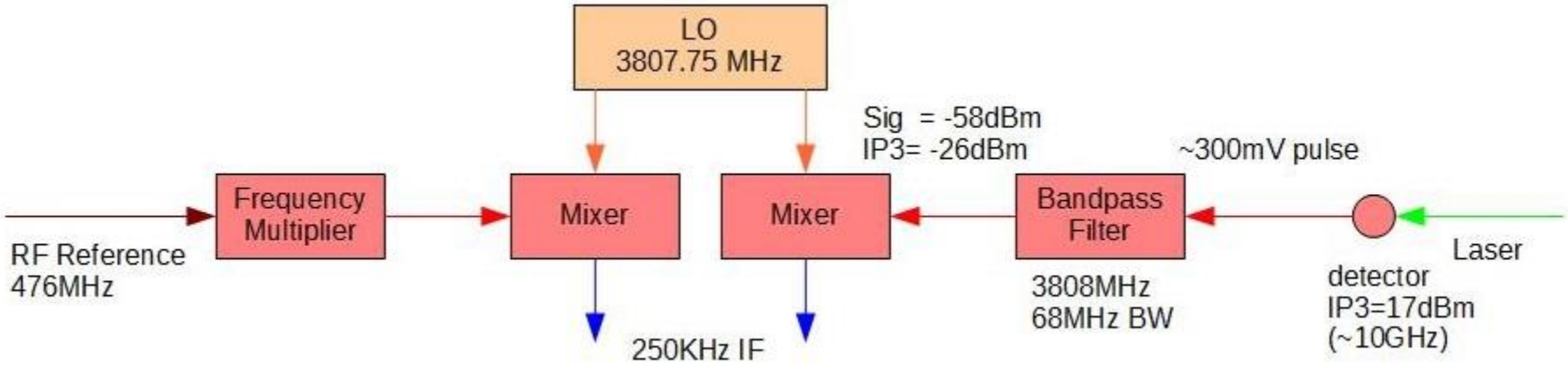
Ringing filter reduces signal amplitude – Next Slide

Frequency Selection and Diode Ringing Filter

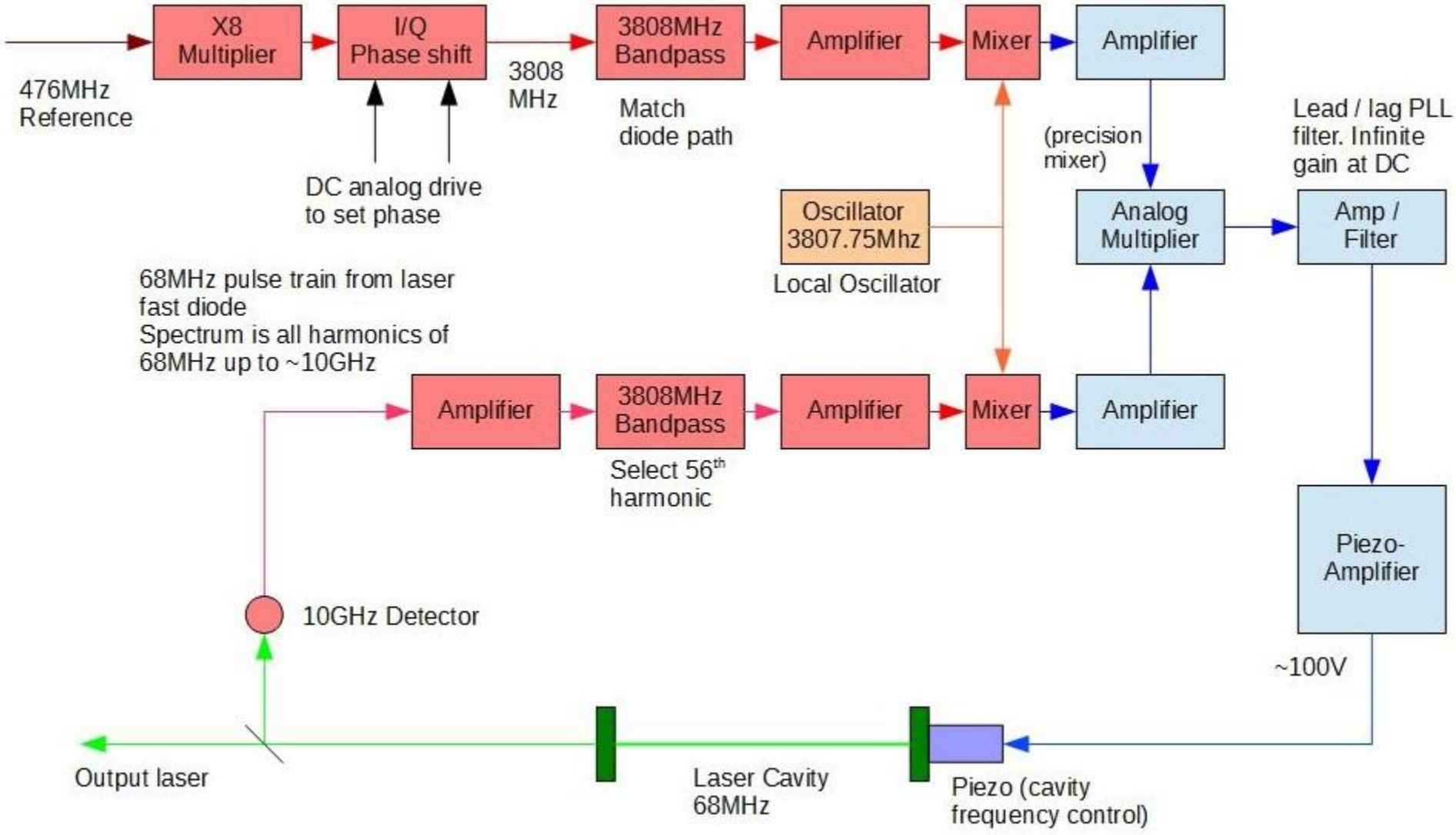
- In principal not needed, but this greatly reduces the dynamic range on the mixer.
- Typically design filter bandwidth to be similar to the laser repetition rate.
- Signal amplitude (and IP3) reduced by the ratio of the diode bandwidth to the filter bandwidth.
  - X10 bandwidth reduction is 20dB signal loss.
- Higher locking frequency gives better phase detector performance, but needs narrower filter, and there may be practical issues with PC board electronics.
- SLAC picked 3808 MHz, 56 X 68MHz laser frequency.
  - 8X our 476MHz reference frequency – easy to generate
  - Works on standard FR4 PC boards
  - 1.7% bandwidth reasonable for commercial ceramic filters.

SLAC Locker – Block Diagram / Frequencies

- [Signal – IP3] ~32dBm -> 64dB linearity
- With a 10dB noise figure, S/N in 10KHz bandwidth is 64dB
  - Design noise figure is 3dB, but cable losses etc. make it worse.
- Corresponds to 23fs RMS at 3808 MHz



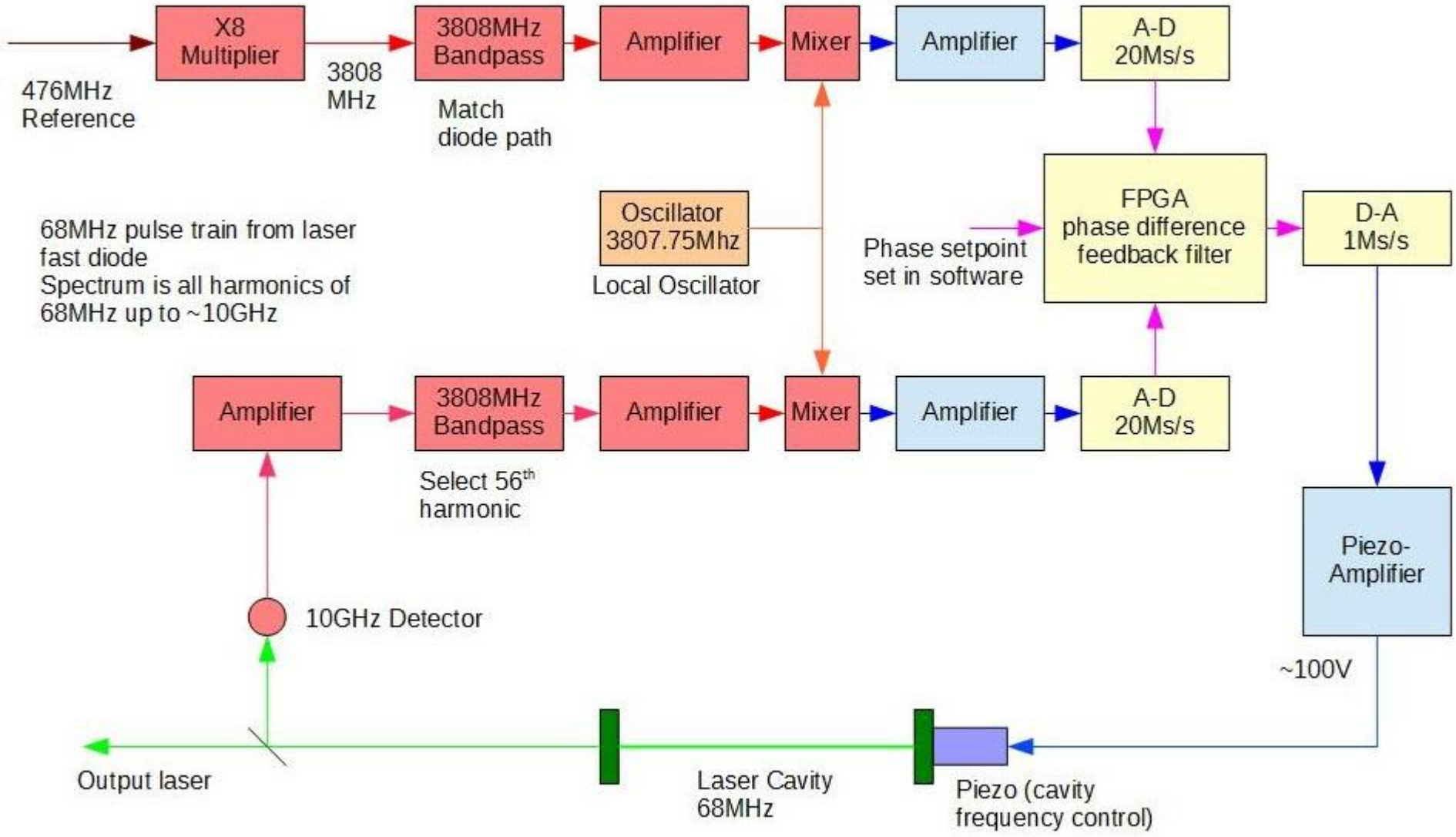
SLAC Analog Locker (ASTA UED)



Analog Locker Notes

- Used analog multiplier as a precision mixer for IF.
  - Simple and good performance but….
  - High input signal levels +/-10V limited IF frequency to ~250KHz to have high linearity IF amplifiers
  - Limited dynamic range requires careful adjustment of all signal levels
- Timing control achieved with 3808MHz I/Q phase shifter
  - Plagued by calibration problems
- Installed on 10 SLAC laser systems, in use for ~1 year.
- Routinely achieved 25-50fs RMS noise.
- ADC / FPGA / DAC system better, but didn't have the available manpower.

SLAC Digital Locker

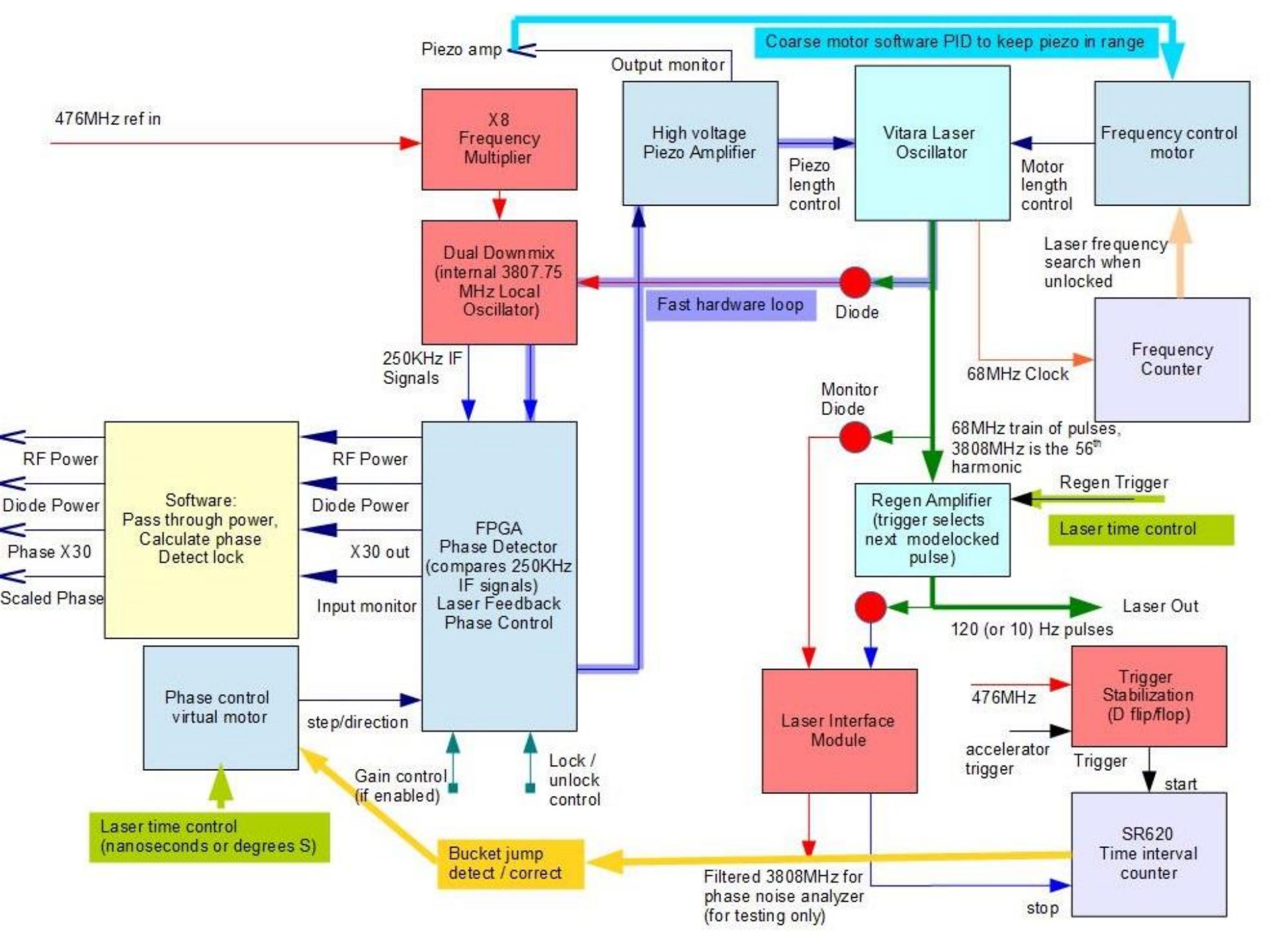


Digital Locker Notes

- Replace analog phase detector and feedback with a ADC / FPGA / DAC
  - 20Ms/s 16 bit ADC, 1Ms/s 18 bit DAC
  - Kintex FPGA – Xilinx Vivado, Matlab System Generator environment
- Simple, low performance (by modern standards) but plenty for this application.
- Use 250KHz IF for backwards compatibility but expect to move to ~1MHz in future
- Phase control now done in FPGA firmware
  - Subtract reference phase from diode phase and compare with set point.
- Typically close laser loop at 6KHz bandwidth
- NOTE: Clocks and IF operate UNLOCKED.

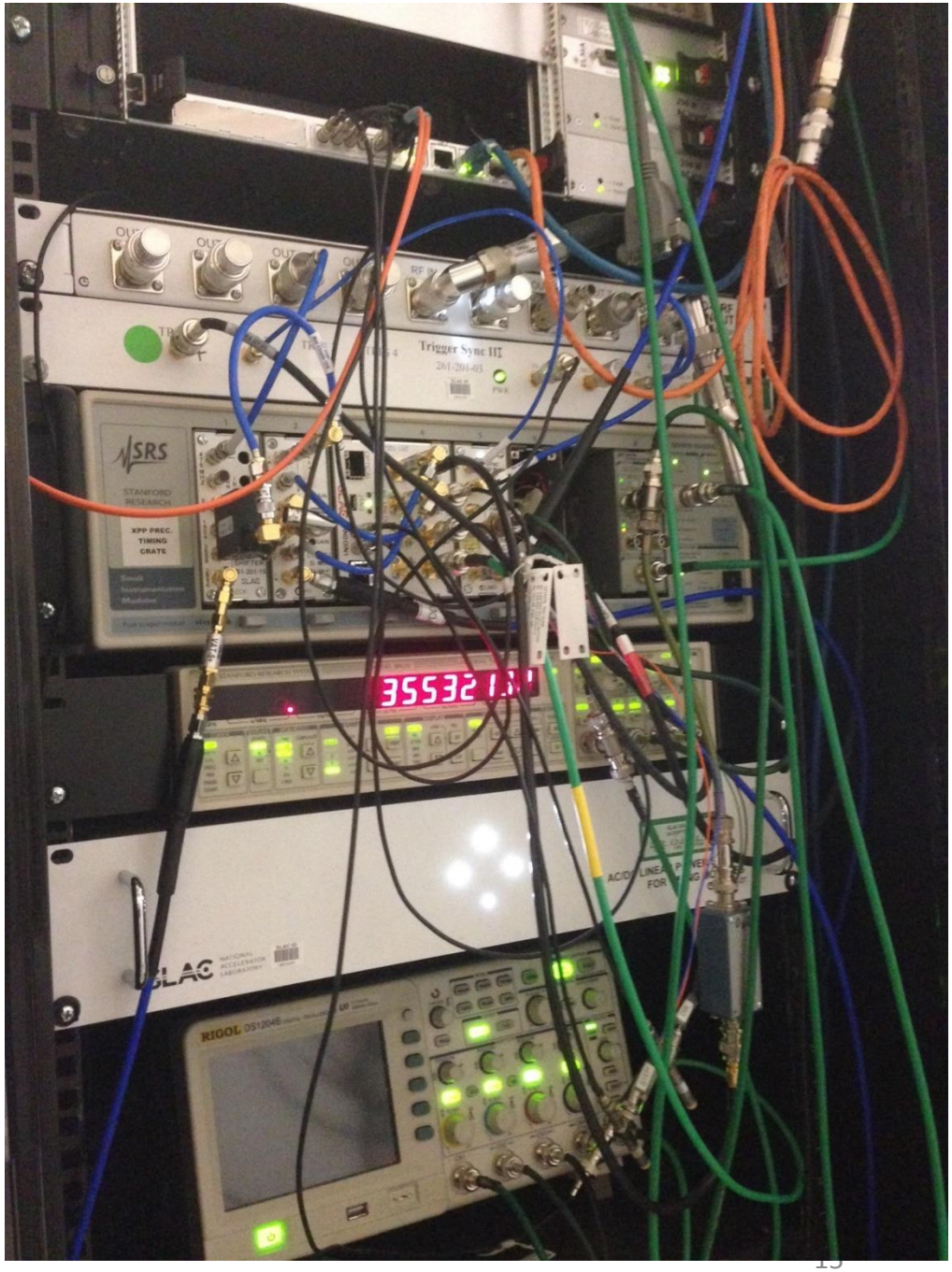
More Than Just the Locker

- Phase control interface
  - SLAC uses a stepper motor like device that interfaces to EPICS.
- Trigger control for regen amp.
  - Need to change regen trigger time for timing changes that are not small compared to oscillator round trip time
  - Use Coherent “SDG” that synchronizes regen triggers to mode-locked laser phase to prevent laser damage!
- Bucket jump detection:
  - 56 cycles of 3808MHz in a 68MHz oscillator cycle – possible for laser to lock to any of the 3808 cycles.
  - Use precision time interval counter to check for bucket jumps
  - Software to rotate phase control phase shift to fix time (up to 56 cycles rotation)
- Laser cavity length control to keep piezo in range.
- Calibration: Determine phase control time when you switch to a different regen amplifier eject pulse.
- Python code to manage all the controls
- EPICS application.
- **This was a lot more work than the RF locker itself!**


Coarse motor software PID to keep piezo in range
Piezo amp
Output monitor
476MHz ref in
X8
Frequency
Multiplier
High voltage
Piezo Amplifier
Vitara Laser
Oscillator
Frequency control
motor
Piezo
length
control
Motor
length
control
Laser frequency
search when
unlocked
Dual Downmix
(internal 3807.75
MHz Local
Oscillator)
Fast hardware loop
Diode
Frequency
Counter
68MHz Clock
250KHz IF
Signals
Monitor
Diode
68MHz train of pulses,
3808MHz is the 56th
harmonic
Regen Trigger
Regen Amplifier
(trigger selects
next modelocked
pulse)
Laser time control
RF Power
Diode Power
Phase X30
Scaled Phase
Software:
Pass through power,
Calculate phase
Detect lock
RF Power
Diode Power
X30 out
Input monitor
FPGA
Phase Detector
(compares 250KHz
IF signals)
Laser Feedback
Phase Control
Laser Out
120 (or 10) Hz pulses
Phase control
virtual motor
step/direction
Laser Interface
Module
476MHz
Trigger
Stabilization
(D flip/flop)
accelerator
trigger
Trigger
start
Gain control
(if enabled)
Lock /
unlock
control
Laser time control
(nanoseconds or degrees S)
Bucket jump
detect / correct
SR620
Time interval
counter
Filtered 3808MHz for
phase noise analyzer
(for testing only)
stop

Hardware

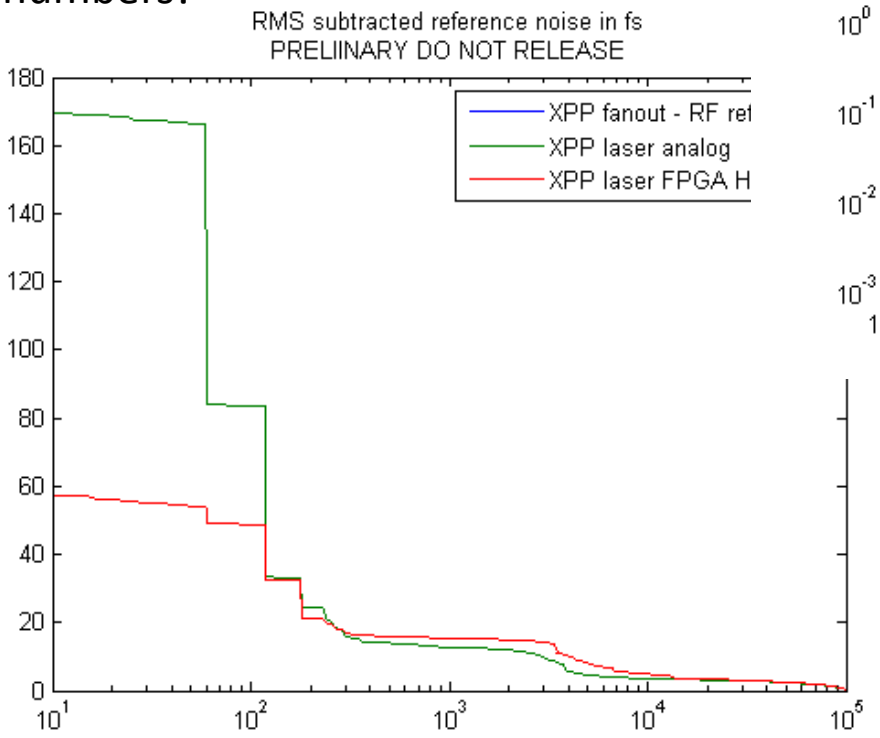
- Use SRS “SIM” crate
  - Convenient mounting and power supplies
- Simple PC board RF electronics
  - Built using ExpressPCB.
- Costs ~$50K to build a locker
- 9 systems in use at SLAC
- Good uptime with minimal intervention.

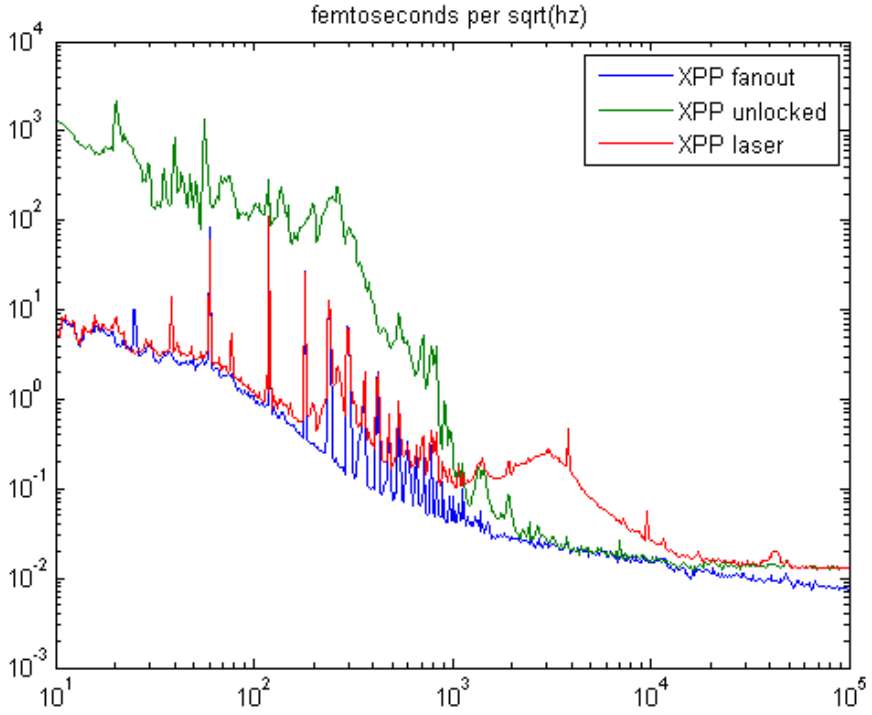


How well does it work?

Measured with Agilent signal source analyzer using an independent diode

Reference noise dominates below 100Hz so we are subtracting big numbers!





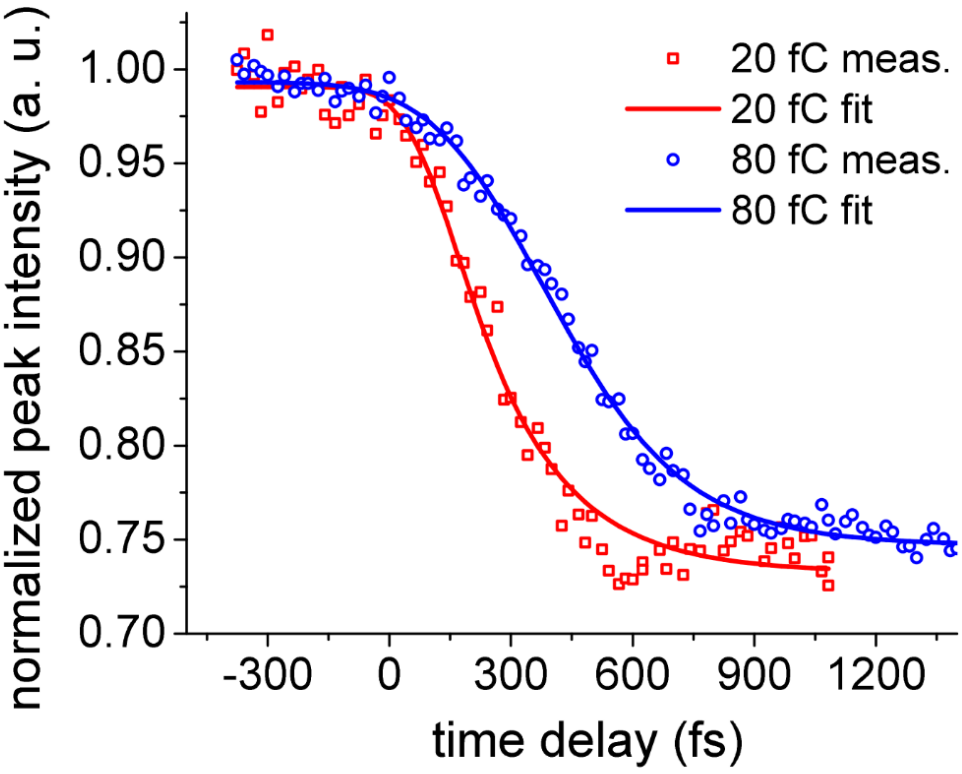
Noise is below 60fs RMS, based on in-loop measurements and bandwidth limited measurements think we have ~25fs RMS

Very close to calculated noise!

Time resolved diffraction measurement

~100fs resolution in diffraction timing experiment at ASTA UED.

Non-thermal melting in Bi



Renkai Li, SLAC ASTA UED system

How to build RF Laser Locking Systems

- CHECK RF SIGNAL LEVELS
  - Balance nonlinearity [2X(IP3 – signal)] against noise (10dB above thermal in the system bandwidth) at ALL stages in the locking system.
  - You avoid 99% of all RF design mistakes with just this rule!
- Work at a few GHz.
  - Generally not worth pushing to ultra-high frequencies.
- Use a heterodyne system.
  - Saves you from DC drift IP2 nonlinearity issues
- Use a ADC / FPGA / DAC
  - We learned the hard way that analog is more trouble than its worth.
- Be careful about acoustic noise in the laser room – mode-locked lasers are extremely sensitive.
- Pick parts for good linearity (IP3). This is usually more critical than noise figure.
  - No need for exotic parts – mass vendors like MiniCircuits make parts that are within a factor of 2 of the best available.
- CHECK RF SIGNAL LEVELS

This is a job for Engineers, not Students (and not Scientists!).

Its like building a bridge – you don't want to have to re-invent engineering!

How to do better?

- High performance diode has 2X bandwidth, 20dB better IP3
  - Scaling isn't simple, but probably X2-X4 improvement
- Higher IF frequency will reduce the group delay in the filter and allow higher bandwidths
- Fiber lasers have much lower noise, so we need a lower bandwidth loop -> less integrated noise
- Drift – typically dominated by cables, so would need temperature controlled runs everywhere
  - Temperature coefficient is typically 1e-5/DegC. 30fs/M/degC.
- In many RF UED applications, you may be limited by the gun or buncher RF system.